A SOLID-STATE CIRCUITS SOCIETY da IEEE

Capítulo Sul BRAZIL convida para a Série de Palestras promovidas pela IEEE e pelo INSTITUTO DE INFORMÁTICA da UFRGS.

IEEE Série de PALESTRANTES em Microeletrônica – Circuitos Integrados . Série "DISTINGUISHED LECTURERS" da IEEE.

DATA: 24/Setembro 3a. feira
Local: INSTITUTO de INFORMÁTICA
Universidade Federal do Rio Grande do Sul
Campus do Vale – Prédio 67 / Auditório
Av. Bento Goncalves 9500 PORTO ALEGRE, BRASIL

Lecture 1
Prof. Jacob Baker
University of Nevada, Las Vegas (USA)
Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design
10.00-11.00 hs
Lecture 2
Prof. Jacob Baker
A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion
11.00-12.00 hs

Lunch Break / Intervalo - Almoço

Lecture 3
Prof. Vladimir Stojanovic
University of California, Berkeley (USA)
Designing Future VLSI Systems with Monolithically Integrated Silicon-Photonics
14.00-16.00 hs

Coffee break
Lecture 4
Dr. Alvin Loke
Qualcomm Technologies (USA)
IC Technology at New Nodes Made Easy
16.30-18.30 hs

DISTINGUISHED LECTURERS – SOLID-STATE CIRCUITS SOCIETY

Distinguished Lecturer : RUSSEL JACOB (Jake) BAKER

Biography:

Russel Jacob (Jake) Baker (S'83-M'88-SM'97-F'13) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas, in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno in 1993. His Google scholar profile is located at http://cmosedu.com/jbaker/pictures/rjacobbaker12_high_res.jpg

From 1981 to 1987 he served in the United States Marine Corps Reserves. From 1985 to 1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada test site. During this time he designed over 30 electronic and electro-optic instruments including high-speed fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, Pockell's cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1993 to 2000 he served on the faculty in the department of electrical engineering at the University of Idaho. In 2000 he joined a new electrical and computer engineering program at Boise State University where he served as department chair from 2004 to 2007. At Boise State he helped establish graduate programs in electrical and computer engineering including, in 2006, the university's second PhD degree. In 2012 he joined the faculty at the University of Nevada, Las Vegas where his research focuses on integrated electrical/biological circuits and systems, methods to fabricate trusted integrated circuits, and the delivery of online engineering education. Since 1993 he has also consulted for various companies and laboratories including: Aerius Photonics, Amkor, Agere, Arete' Associates, ASUS, Atmel, Cirque, Contour Semiconductor, Dell, Elm Technology, Elpida, FLIR, Fujitsu, Infineon, InvenSense, ITRAN Communications, Kingston Technology, the Lawrence Berkeley Laboratory, Lockheed-Martin, LSI, Micron, Nascentric, OmniVision, Oracle, Rendition, Samsung, SK Hynix, Sun, Tower Semiconductor, and Xilinx.

Professor Baker holds over 200 granted or pending patents in integrated circuit design. Among his inventions is the *K*-Delta-1-Sigma modulator topology used in the Baker analog-to-digital converter. He is a member of the electrical engineering honor society Eta Kappa Nu, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books *CMOS Circuit Design, Layout, and Simulation*, *CMOS Mixed-Signal Circuit Design*, and a coauthor of *DRAM Circuit Design: Fundamental and High-Speed Topics*. He received the 2000 Best Paper Award from the IEEE Power Electronics Society, the 2007 Frederick Emmons Terman Award, and the 2011 IEEE Circuits and Systems (CAS) Education Award.

He also currently serves, or has served, as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau (2007-present), as editor for the Wiley-IEEE Press Book Series on

Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-present), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University (2012-present), as the Technology Editor for the *IEEE Solid-State Circuits Magazine* (2012-present), and as a Distinguished Lecturer for the SSCS (2013-present).

Distinguished Lecturer : VLADIMIR MARKO STOJANOVIC

Biography:

Vladimir Stojanovic is an Associate Professor of Electrical Engineering and Computer Science at University of California, Berkeley. His research interests include design, modeling and optimization of integrated systems, from CMOS-based VLSI blocks and interfaces to system design with emerging devices like NEM relays and silicon-photonics. He is also interested in design and implementation of energy-efficient electrical and optical networks, and digital communication techniques in high-speed interfaces and high-speed mixed-signal IC design.

Vladimir received his Ph.D. in Electrical Engineering from Stanford University in 2005, and the Dipl. Ing. degree from the University of Belgrade, Serbia in 1998. He was also with Rambus, Inc., Los Altos, CA, from 2001 through 2004 and with MIT as Associate Professor from 2005-2013. He received the 2006 IBM Faculty Partnership Award, and the 2009 NSF CAREER Award as well as the 2008 ICCAD William J. McCalla, 2008 IEEE Transactions on Advanced Packaging, and 2010 ISSCC Jack Raper best paper awards. He is an IEEE Solid-State Circuits Society Distinguished Lecturer for the 2012-2013 term.

Talk Title:

"Designing Future VLSI Systems with Monolithically Integrated Silicon- Photonics "

Abstract: Chip design is radically changing. This period of change is a very exciting time in integrated circuit and system design. On one hand, cross-layer design approaches need to be invented to improve system performance despite CMOS scaling slowdown. On the other, a variety of emerging devices are lined-up to extend or potentially surpass the capabilities of CMOS technology, but require key innovations at the integration, circuits and system levels.

This lecture describes how monolithic integration of photonic links can revolutionize the VLSI chip design, dramatically improving its performance and energy-efficiency. Limited scaling of both on-chip and off-chip interconnects, coupled with CMOS scaling slowdown have led to energy-efficiency and bandwidth density constraints that are emerging fast as the major performance bottlenecks in embedded and high-performance digital systems. While optical interconnects have shown promise in extensive architectural studies to date, significant challenges need to be overcome both in device and circuit design as well as the integration strategy. We illustrate how our cross-layer approach guides the system design by connecting process, device and circuit

optimizations to system-level metrics, exposing the inherent trade-offs and design sensitivities. Our experimental platforms demonstrate the technology potential at the system level and provide feedback to modeling and device design. In particular, we'll describe the recent breakthroughs in monolithic photonic memory interface platform with fastest and most energy-efficient modulators demonstrated in a 45nm process node. Based on these design principles and technology demonstrations, we project that in the next decade tailored hybrid (electrical/optical) integrated systems will provide orders of magnitude performance improvements at the system level and revolutionize the way we build future VLSI systems. Moreover, just like integrating the inductor into CMOS at the end of 1990s revolutionized the RF design and enabled mobile revolution, integration of silicon-photonic active and passive devices with CMOS is greatly positioned to revolutionize a number of analog and mixed-signal applications – low-phase noise signal sources and large bandwidth, high-resolution ADCs, to name a few.

Distinguished Lecturer : ALVIN LOKE

Biography:

Alvin Loke received his BASc degree from University of British Columbia, and MSEE and PhDEE degrees from Stanford University. His doctoral work focused on copper interconnects with low-K polymer dielectrics. From 1998 to 2001, he worked on CMOS technology integration at HP Labs and then at Chartered Semiconductor Manufacturing as an Agilent assignee. In 2001, he transferred to Fort Collins, Colorado where he designed CMOS PLL circuits for embedded SerDes and ASIC core clocking. From 2006 to 2013, he was with Advanced Micro Devices where he designed high-speed link electrical/optical circuits and addressed analog/mixed-signal concerns for next-generation CMOS. He recently joined Qualcomm where he works on mobile DDR signal integrity and finFET transceiver design. Alvin has authored 40 publications and holds 13 US patents. He served on the CICC technical program committee and as Guest Editor of the IEEE Journal of Solid-State Circuits. He was an active Solid-State Circuits Society chapter officer in Fort Collins for 10 years.

Talk: *Integrated Circuits Technology at New Nodes Made Easy*

Abstract:
Despite increasing economic and technical challenges to scale CMOS, we continue to witness unprecedented performance with 22-nm fully-depleted tri-gate devices now well in production. This tutorial seminar offers a summary of how CMOS device technology has progressed over the past two decades. We will review MOS device and short-channel fundamentals to motivate how device architectures in production have evolved to incorporate elements such as halos and spacers, mechanical strain engineering, high-K dielectric and metal gate, fully-depleted device architectures and finally, tri-gate finFETs.