Seminar

"Ultra-low power logic circuits: from voltage-mode to current-mode"

Speaker: Prof. Massimo Alioto

(IEEE CAS Distinguished Lecturer)

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TALK TITLE: Ultra-low power logic circuits: from voltage-mode to current-mode

SPEAKER INFO:

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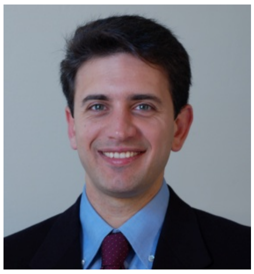

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SPEAKER SHORT BIO:

Massimo Alioto (M'01–SM'07) was born in Brescia, Italy, in 1972. He received the laurea degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively. In 2002, he joined the Dipartimento di Ingegneria dell'Informazione (DII) of the University of Siena as a Research Associate and in the same year as an Assistant Professor. In 2005 he was appointed **Associate Professor** of Electronics, and was engaged in the same faculty in 2006. In the summer of 2007, he was a Visiting Professor at EPFL - Lausanne (Switzerland). In 2009-2010, he is **Visiting Professor** at BWRC – UCBerkeley, investigating on ultra-low power circuits and wireless sensor nodes.

Since 2001 he has been teaching undergraduate and graduate courses on advanced VLSI digital design, microelectronics and basic electronics. He has authored or co-authored more than 140 **publications** on journals (50+, mostly IEEE Transactions) and conference proceedings. Two of them are among the 25 most downloaded TVLSI papers in 2007 (respectively 10th and 13th). He is co-author of the **book** Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL and SCL Digital Circuits (Springer, 2005). His primary research interests include the modeling and the optimized design of CMOS high-performance, low-power and ultra low-power digital circuits, arithmetic and cryptographic circuits, interconnect modeling, design/modeling for variability-tolerant and low-leakage VLSI circuits, circuit techniques for emerging technologies. He is the director of the Electronics Lab at University of Siena (site of Arezzo).

Prof. Alioto is an **IEEE Senior Member** and a member of the HiPEAC Network of Excellence. He is the **Chair Elect** of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society, for which he is also **Distinguished Lecturer**. He is regularly invited to give talks and tutorials to academic institutions, conferences and companies throughout the world. He has served as a member of various conference **technical program committees** (ISCAS, PATMOS, ICM, ICCD, CSIE) and Track Chair (ICECS, ISCAS, ICM, ICCD). He serves as **Associate Editor** of the IEEE Transactions on VLSI Systems, as well as of the Microelectronics Journal, the Integration – The VLSI journal and the Journal of Circuits, Systems, and Computers. He is **Guest Editor** of the Special Issue "Advances in oscillator analysis and design" of the Journal of Circuits, Systems, and Computers (2009).

ABSTRACT

In the last years, subthreshold CMOS logic circuits have become very popular in ultra-low power applications, which typically constrain the power budget to a few tens of μWs and the supply voltage to a few hundreds of mV. Designing at such low power/voltage is challenging and requires a deep understanding of the power-delay tradeoff, as well as of the impact of design variables and variability sources on the circuit robustness.

In this talk, a survey of recent design techniques for ultra-low power logic circuits is presented. Traditional voltage-mode logic styles are discussed, and their limitations in subthreshold regime are highlighted. The effect of interdie and intradie process variations is analyzed, and design techniques are discussed at the physical, transistor, gate and system level of abstraction. Detailed guidelines on how to build ultra-low power standard cell libraries are derived, and examples are provided. A detailed comparison of design flows targeting standard and subthreshold CMOS logic is also presented to understand how to specifically build design flows for ultra-low power.

Current-mode logic styles are then analyzed, and their advantages in terms of minimum energy per operation are discussed. Design issues arising in the ultra-low power realm with a power consumption in the order of pW-per-gate are discussed, and appropriate circuit techniques to allow reliable operation are presented. Limits to ultra-low power operation are analyzed by evaluating the minimum supply voltage that is allowed in MCML circuits, and recent body biasing techniques to push down this voltage limit are discussed. The impact of process/voltage/temperature variations is analyzed to understand the intrinsic advantages of MCML circuits in ultra-low power circuits, and design strategies to counteract power-delay variations are presented.

Successful designs and state-of-the-art chips are presented to gain a clear understanding of the state-of-the-art, and which direction the research is moving to. Finally, open questions and aspects that require further investigation and new directions are discussed.

KEYWORDS

Ultra-low power, subthreshold CMOS logic, MOS Current Mode Logic, minimum-energy operation, VLSI design, PVT variability