As technology scales, effects such as NBTI increase their importance. The performance degradation in CMOS circuits caused by NBTI is being studied for many years and several models are available. In this work, an equivalent circuit representing one of these models is presented and evaluated through electrical simulation. The proposed circuit is process independent once the chosen model does not present any relation to technology parameters. Experimental results indicate that the equivalent circuit is valid to evaluate the degradation of PMOS transistors due to aging. Using the proposed circuit, threshold voltage degradation of each transistor may be simulated individually, which allows the evaluation of complex CMOS gates in a linear cost in relation to the number of transistors.

Introduction

As semiconductor manufacturing migrates to more advanced deep-submicron technologies, accelerated aging effect becomes one major limiting factor in circuit design. This is a challenge for designers to effectively mitigate degradation and improve the system lifetime. One of the most important phenomenon that causes temporal reliability degradation in MOSFETs is the Negative Bias Temperature Instability (NBTI) (1).

NBTI is an effect that leads to the generation of interface Si/SiO$_2$ traps, causing consequently a shift in the PMOS transistor threshold voltage ($V_{th}$), being dependent on the operating temperature and exposure time. This effect induces a performance degradation, increasing the signal propagation delay in the circuit paths. Besides, it degrades the drive current and the noise margin. Although it is known since a long time (2), only in nano-scale designs it has been identified as a critical reliability issue (3) due to the increase of both gate electrical fields and chip operation temperature, combined with the power supply voltage reduction.

Recently, much effort has been expended to further the basic understanding of this mechanism (4). In order to estimate the threshold voltage degradation caused by NBTI, different analytical models have been proposed in literature (3), (5), (6)-(10). Moreover, some of these models are somewhat difficult to be used once specific and empirical process parameters are required.

In order to have an estimative about circuit failure, electrical simulation may be performed applying one of those models represented by an equivalent electrical circuit. In this paper, it is demonstrated the use of the R-D model, proposed in (5), which describes the dependence between physical and environmental factors. The main goal is to validate the equivalent circuit proposed to represent the NBTI R-D model. It is used to evaluate the threshold voltage degradation of each transistor independently, demonstrating its
usefulness for CMOS complex gates evaluation in a linear cost in relation to the number of transistors.

This paper is structured as follows: the Modeling section describes in details the R-D model; the Equivalent Circuit section presents the model implementation; the Experimental Results section discusses some electrical simulation results; and, in the Conclusion section, the results and future works are outlined.

**Modeling**

Although the first experiments on NBTI reports to late 60’s, only in late 70’s a comprehensive study of available experiments was performed. Jeppson (11) presents a generalized Reaction-Diffusion model, being the first one to discuss the role of relaxation and bulk traps.

As NBTI was not an issue on NMOS technology at that time, no much research on this field was performed until early 90’s. Increased field and temperature due to the technology scaling reintroduces NBTI concerns for both analog and digital circuits. Several works proposed different models based on the Reaction-Diffusion model presented by Jeppson (3), (5), (6)-(10). Those models are usually empirical and related to specific technologies, therefore they are quite difficult to implement for circuit simulation and particularly hard to be compared among themselves and with others.

A general and accurate analytical model was presented by Vattikonda et al. (5). It is based on the physical understanding and published experimental data for both DC and AC operations. This model can be appropriately customized and implemented into an equivalent electrical circuit, allowing to perform Spice simulations analysis.

It is strongly believed that when a gate voltage is applied, it initiates a field-dependent reaction at the Si/SiO₂ interface, that generates interface traps (N_{it}) by breaking the passivated Si-H bonds (6),(3),(9),(10). These traps appear because of the positive holes from the channel that cause the diffusion away of the H, provoking the increase of V_{th}. The dependence between V_{th} and N_{it} can be noted by:

\[ \Delta V_{th} = \frac{qN_{it}}{C_{ox}} \]  

where C_{ox} is the oxide capacitance per unit area.

During the operation of PMOS device, there are two different phases of the NBTI effect, depending on the bias condition: stress and recovery. During the stress phase, when V_{SG}=V_{DD}, positive interface traps are accumulating and H diffuses away, and in the recovery phase, when the V_{GS}=0V, the H diffuses back and anneals the broken Si-H, recovering the NBTI degradation (5). The stress phase is also known as static phase.

The NBTI effect can be modeled as ‘static’ or ‘dynamic’ operation. The static one presents only the stress phase because it is required that the gate stays only negative biased during all the time. But, in actual circuit operations, where gate voltage switches between 0V and V_{DD}, both stress and recovery phases occur, denoting the dynamic operation.
For the direct calculation of $V_{th}$ variation under NBTI, the Vattikonda’s model has been adopted in this work (5). The formulation for stress phase is:

$$\Delta V_{th} = \sqrt{K_v} \cdot (t - t_0)^{1/2} + \Delta V_{th0}^{2} + \delta_v$$

being

$$K_v = \frac{A \cdot \sqrt{C_{ox} \cdot (V_{GS} - V_{th})}}{1 - \frac{V_{DS}}{\alpha(V_{GS} - V_{th})}} \exp \left( \frac{E_{av}}{E_0} \right) \exp \left( \frac{-E_v}{kT} \right)$$

and for recovery phase, the following equation is used:

$$\Delta V_{th} = \left( \Delta V_{th0} - \delta_v \right) \left[ 1 - \sqrt{\eta(t - t_0) / t} \right]$$

These models are scalable with target process and design parameters, such as gate oxide thickness ($t_{ox}$), gate-source ($V_{GS}$) and drain-source ($V_{DS}$) transistor voltages, device threshold voltage ($V_{th}$), temperature ($T$) and time ($t$). In Table I, the default values of Vattikonda’s model coefficients are given for 45 nm PTM process (12). We refer the reader to reference (5) for further details on the model.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>1.8 mV/nm/C$^{0.5}$</td>
</tr>
<tr>
<td>$\eta$</td>
<td>0.35</td>
</tr>
<tr>
<td>$E_0$</td>
<td>2.0 MeV/cm</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>1.3</td>
</tr>
<tr>
<td>$\delta_v$</td>
<td>5.0 mV</td>
</tr>
<tr>
<td>$E_a$</td>
<td>0.13 eV</td>
</tr>
</tbody>
</table>

In fact, the stress and recovery processes are somewhat more complex. They may involve oxide traps and other charged residues (9), (13–15). These non-H based mechanisms may have faster response time than the diffusion process. Without losing generality, their impact can be included as a constant of $\delta_v$ (5).

Mathematical simulation results of $V_{th}$ degradation using the formulas presented above are shown in Figure 1 for both (a) static and (b) dynamic NBTI.

Figure 1. Results of the simulation of static (a) and dynamic (b) NBTI presented in (5).
In real circuits, transistors are excited in different moments, for a different given amount of time. Therefore, each transistor will suffer distinct aging speed. This work presents the development of an equivalent electrical circuit representation to the analytical model proposed by Vattikonda et al. (5), and its application in electrical simulation evaluating the aging effect of every PMOS transistor on the circuit. For each PMOS transistor, the NBTI effect is calculated and its degradation evaluated.

![Figure 2. Equivalent electrical circuit for Vattikonda’s NBTI model.](image)

In order to implement the threshold voltage variation ($\Delta V_{\text{th}}$) presented in Equations (2) and (5), it is proposed the circuit shown in Figure 2. As every transistor is evaluated individually, it is not possible to apply the degradation calculation as a parameter to the used model card (global process parameters for all devices under simulation). Thus, individual device threshold voltages variation are controlled by modifying individual source-bulk transistor voltage ($V_{SB}$), according to (16):

$$V_{\text{th}} = V_{\text{th}0} + \gamma \left( \sqrt{\Phi_x + V_{SB}} - \sqrt{\Phi_z} \right)$$  \hspace{1cm} [5]

The $V_{BS}$ of every transistor is represented as a dependent source of the potential at node ‘x’ in Figure 2. The voltage sources, $\Delta V_{\text{th}_s}$ and $\Delta V_{\text{th}_r}$, represent values dependent of the variables that are present on each NBTI phase. The values $\Delta V_{\text{th}_s}$ and $\Delta V_{\text{th}_r}$ are calculated according to the stress and the recovery Equations (2) and (4), respectively. The resultant equations implemented in these sources are:

$$\Delta V_{\text{th}_s} = \sqrt{K_v \cdot (t-t_0)^{5/2} + V(z)^2 + \delta_v}$$  \hspace{1cm} [6]

being

$$K_v = A \cdot \alpha \cdot \sqrt{C_{\alpha} \left( \Delta V_{GS} - V_{th} \right)} \left[ \frac{1 - \frac{V_{DS}}{\alpha (\Delta V_{GS} - V_{th})}}{\beta} \right] \exp \left( \frac{E_{\alpha}/E_0}{\exp(E_{\alpha}/kT)} \right)$$  \hspace{1cm} [7]

and

$$\Delta V_{\text{th}_r} = (V(y) - \delta_v) \left[ 1 - \frac{(t-t_0)/t}{\sqrt{t}} \right]$$  \hspace{1cm} [8]

The operating time and relaxation time of each transistor is obtained by integrator circuits, implemented by using ideal components (R and C). The voltage between gate and ground...
nodes of the transistor under analysis (V_{CTRL}) controls the activation of the integrator circuit, allowing the measurement of both operation and relaxation times.

Therefore, during the simulation time, the sources $\Delta V_{th,S}$ and $\Delta V_{th,R}$ will provide the values corresponding to the threshold voltage variation. When a gate voltage is applied in a given transistor, the threshold voltage variation is calculated by the circuit and provided through the voltage at node ‘x’, i.e. $V(x)$. V_{CTRL} voltage defines which ideal switch (Sw1-Sw4) is open and closed, allowing the calculation both of stress and recovery phases, independently.

Figure 3 illustrates how the equivalent circuit controls the $V_{BS}$ dependent source, therefore controlling the threshold voltage of the transistor under evaluation. The $\beta$ value stands for the estimated relation between the two interdependent voltages $V_{th}$ and $V_{BS}$.

![Figure 3. CMOS inverter under NBTI aging evaluation.](image)

**Experimental Results**

In order to validate the proposed circuit, HSPICE electrical simulations were carried out in two different CMOS logic gates, an Inverter and a 2-input Nand, being calculated the threshold voltage degradation for each of them. Moreover, the rise transition delay degradation (in comparison with the operation time) was also obtained. For simulations, 45 nm PTM process parameters (12), operating temperature of 100ºC, and supply voltage of 1.1V were taken into account.

For Inverter gate, it was applied an input signal with a duty cycle of 50% ($t_{stress} = t_{recovery}$), during a period enough to evaluate the degradation of PMOS $V_{th}$ in long term regime. In the case of Nand simulation, it was applied two different input signals (different duty cycles - 50% and 25%), one on each input, in order to prove that, using this method, it is possible to calculate the degradation of each transistor individually.

In Figure 4, it is shown the degradation of both logic cells, by presenting $\Delta V_{th}$ behavior. Notice that, on the Nand gate the transistor that was stimulated with 25% duty cycle signal (dotted line in Figure 4b) suffered more degradation than the other input, excited with 50% duty cycle signal (filled line in Figure 4b).
Figure 4. Results obtained by HSPICE simulation of the threshold voltage degradation in Inverter (a) and 2-input Nand (b). The labels $t_{SA}, t_{SB}, t_{RA}$ and $t_{RB}$ are the stress time and the recovery time for both inputs – A and B – respectively.

Threshold voltage degradation and rise transition delay variation are presented in Tables II and III, considering different operating times for Inverter and Nand gates.
### TABLE II. ΔVth degradation after a time operation.

<table>
<thead>
<tr>
<th>Time operation</th>
<th>Inverter</th>
<th>Nand</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Input A</td>
<td>Input B</td>
</tr>
<tr>
<td>1 hour</td>
<td>2.3 %</td>
<td>2.2 %</td>
</tr>
<tr>
<td>1 day</td>
<td>4.4 %</td>
<td>4.4 %</td>
</tr>
<tr>
<td>1 month</td>
<td>9.4 %</td>
<td>9.2 %</td>
</tr>
<tr>
<td>1 year</td>
<td>16.2 %</td>
<td>15.9 %</td>
</tr>
<tr>
<td>5 years</td>
<td>22.7 %</td>
<td>22.3 %</td>
</tr>
</tbody>
</table>

### TABLE III. Rise delay propagation time degradation after a time operation.

<table>
<thead>
<tr>
<th>Time operation</th>
<th>Inverter gate delay (t&lt;sub&gt;rise&lt;/sub&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 hour</td>
<td>1.3 %</td>
</tr>
<tr>
<td>1 day</td>
<td>2.8 %</td>
</tr>
<tr>
<td>1 month</td>
<td>6.4 %</td>
</tr>
<tr>
<td>1 year</td>
<td>11.3 %</td>
</tr>
<tr>
<td>5 years</td>
<td>15.8 %</td>
</tr>
</tbody>
</table>

In order to better visualize the aging effect during a time interval, the results presented in Tables II and III are plotted on the graph presented in Figure 5. The Y axis indicates the percentual threshold voltage degradation while the X axis indicates the elapsed time, from 0 to 5 years of operation.

![Figure 5](image.png)

Figure 5. The aging effect on the transistors during 5 years of operation (for the Inverter and Nand – inputs A and B).

Moreover, a subcircuit containing both the proposed circuit and the PMOS transistor was implemented. Therefore, designers may use this subcircuit instead of the PMOS transistor whenever the NBTI effect evaluation is desirable.

## Conclusions

An equivalent electrical circuit representing the NBTI R-D model, presented by Vattikonda et al. (5), has been proposed. Electrical simulations have demonstrated that it is suitable to predict CMOS cells degradation due to NBTI aging effect, evaluating individually each PMOS transistor at pull-up logic gate network. In future work, more complex CMOS gates, like And-Or-Inverter and Flip-Flops, will be considered.
Acknowledgments

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References